AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-6 (cancelled).

7. (New) A processor, comprising:

a reconfigurable field of data processing cells; and

a register, wherein the register has a data stream memory designed to store at least one of a data stream and parts of the data stream.

8. (New) The processor as recited in claim 7, further comprising:

at least one: i) of a register allocation device to allocate the register, and ii) a register releasing device to release the register.

9. (New) The processor as recited in claim 8, wherein the register allocation device is configured to be preserved over multiple reconfigurations of the reconfigurable field of data processing cells.

10. (New) The processor as recited in claim 7, wherein the register is a RAM PAE.

11. (New) The processor as recited in claim 7, further comprising:

a second register configured to provide read and write access when a virtual FIFO dividing line is implemented.

12. (New) The processor as recited in claim 7, further comprising:

at least one memory unit configured for use as a stack and being configured to indicate at least one of a stack underflow state and a stack overflow state.

13. (New) The processor as recited in claim 12, wherein the at least one measuring unit is configured to indicate the at least one of the underflow state and overflow state of an operating system unit.